




Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(✓) Final Specifications

Module	15.6" (15.55) FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B156HTN01.1 (H/W:0A)
Note ()	R,G phosphor LED Backlight with driving circuit design

Customer	Date
_____	_____
Checked & Approved by	Date
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
<u>Buffy Chen</u>	<u>2013/05/27</u>
Prepared by	Date
<u>HsiangYI CHEN</u>	<u>2013/05/27</u>
NBBU Marketing Division / AU Optronics corporation	



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/11/29	All	Preliminary Edition for Customer		
1.0 2013/01/28	All		Final Edition for Customer	
1.1 2013/02/01	All		Final Edition updated for Customer	
1.2 2013/02/21	19 of 32;23 of 32		Update Mechanical Characteristics	
1.3 2013/05/27	page 28~31		Update EDID(Check Sum:81)	

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B156HTN01.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD (1920(H) x 1080(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B156HTN01.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	15.6" (15.55)			
Active Area	[mm]	344.16 x 193.59			
Pixels H x V		1920x3(RGB) x 1080			
Pixel Pitch	[mm]	0.17925 x 0.17925			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I_{LED}=30mA) (Note: I_{LED} is LED current)	[cd/m ²]	270 typ. (5 points average) 230 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 :1			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	11.0 max. (Include Logic and Blu power)			
Weight	[Grams]	475 max.			
Physical Size Without inverter, bracket.	[mm]		Min.	Typ.	Max.
		Length	358.8	359.3	359.8
		Width	209.0	209.5	210.0
		Thickness	-	-	5.8
Electrical Interface		2 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Anti-glare, Hardness 2H,Haze=42%±7 Reflection type=normal, Reflection≤ 3%			
Support Color		262K colors (RGB 6-bit)			
Temperature Range					
Operating	[°C]	0 to +50			
Storage (Non-Operating)	[°C]	-20 to +60			
RoHS Compliance		RoHS Compliance			



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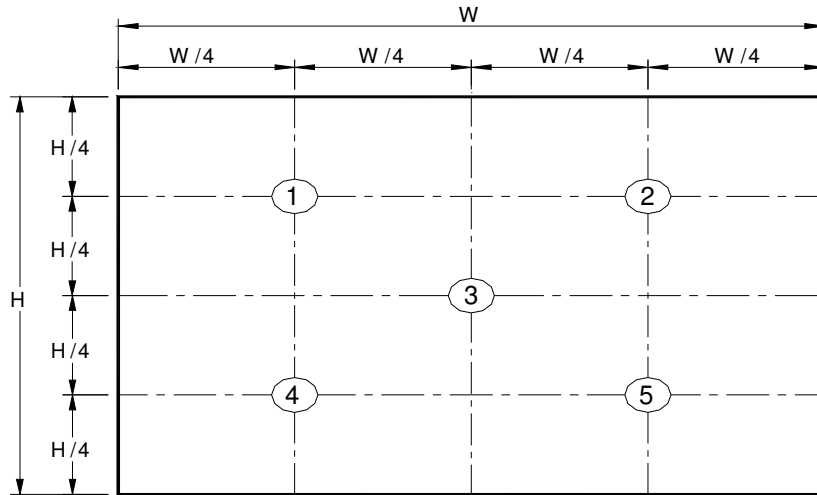
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2.2 Optical Characteristics

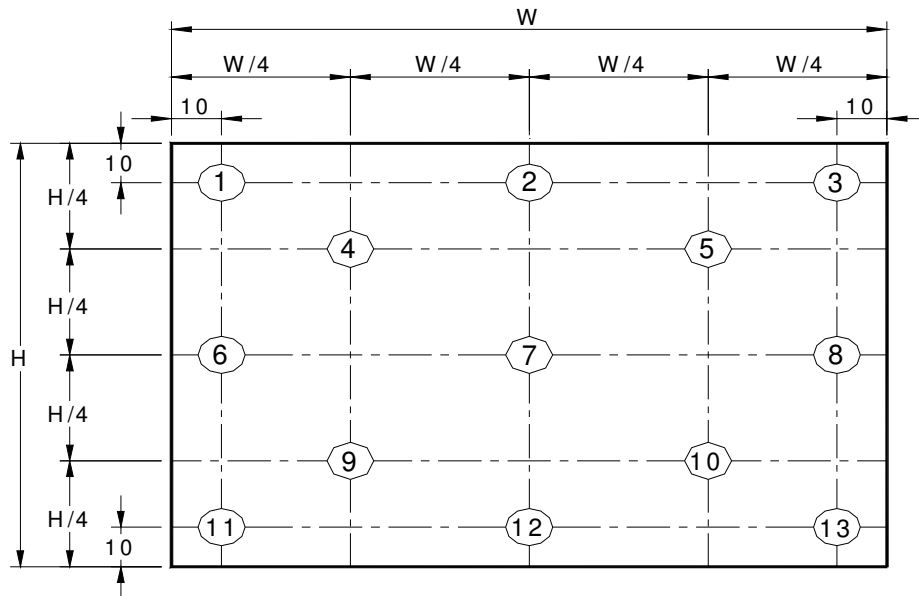
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=30mA			5 points average	230	270	-	cd/m²	1, 4, 5.
Viewing Angle		θ _R	Horizontal (Right) CR = 10 (Left)	60	70	-	degre e	4, 9
		θ _L		60	70	-		
		ψ _H	Vertical (Upper) CR = 10 (Lower)	45	60	-		
ψ _L	50	60		-				
Luminance Uniformity		δ _{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ _{13P}	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio		CR		300	400	-		4, 6
Cross talk		%				4		4, 7
Response Time		T _{RT}	Rising + Falling	-	8	16	msec	4, 8
Color / Chromaticity Coodinates	Red	R _x	CIE 1931	0.646	0.676	0.706	-	4
		R _y		0.283	0.313	0.343		
	Green	G _x		0.187	0.217	0.247		
		G _y		0.631	0.661	0.691		
	Blue	B _x		0.112	0.142	0.172		
		B _y		0.037	0.067	0.097		
	White	W _x		0.283	0.313	0.343		
		W _y		0.299	0.329	0.359		
	NTSC			%		--		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

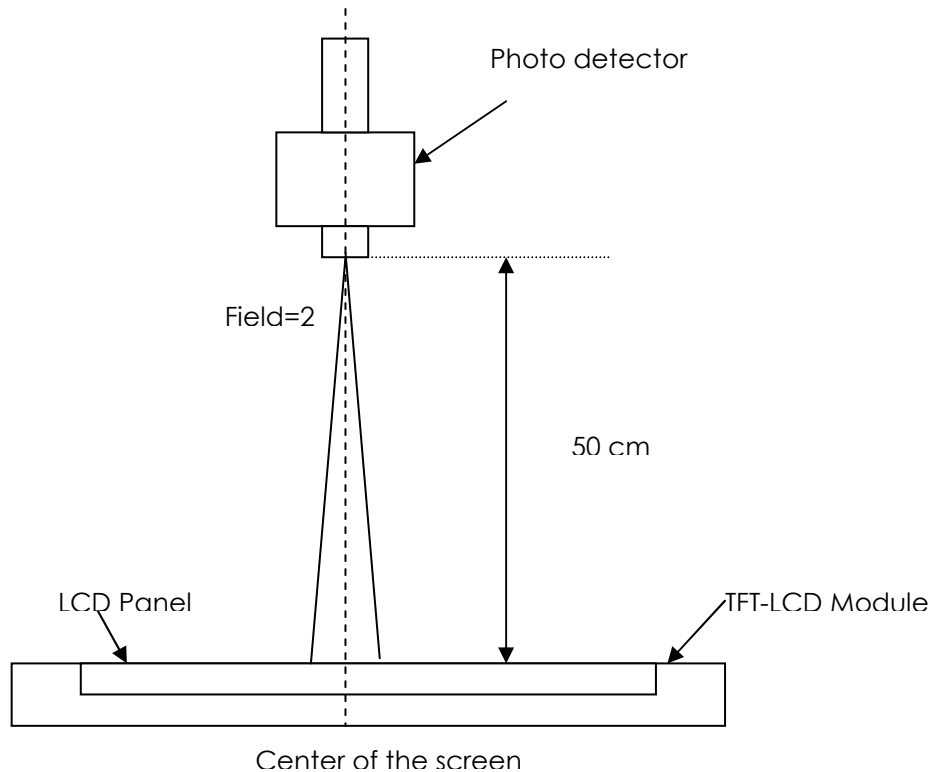
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after

lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points · $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

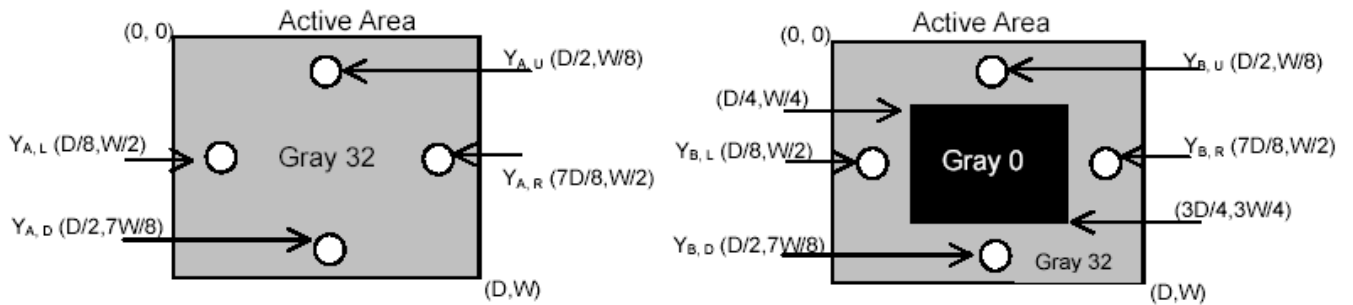
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

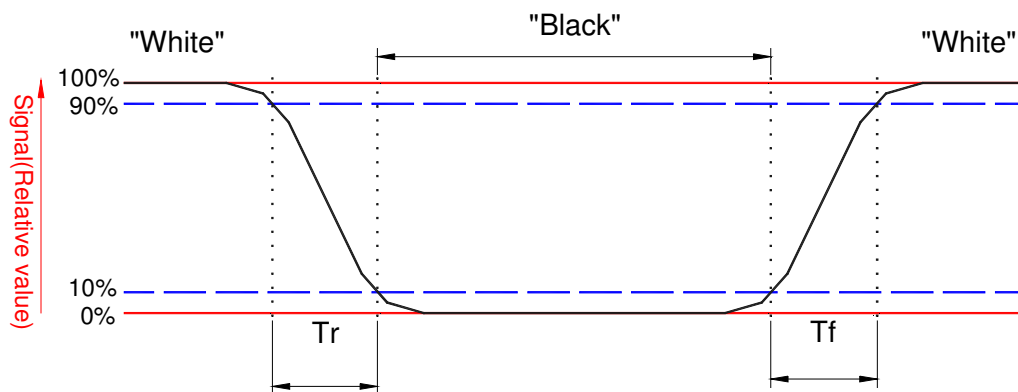
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



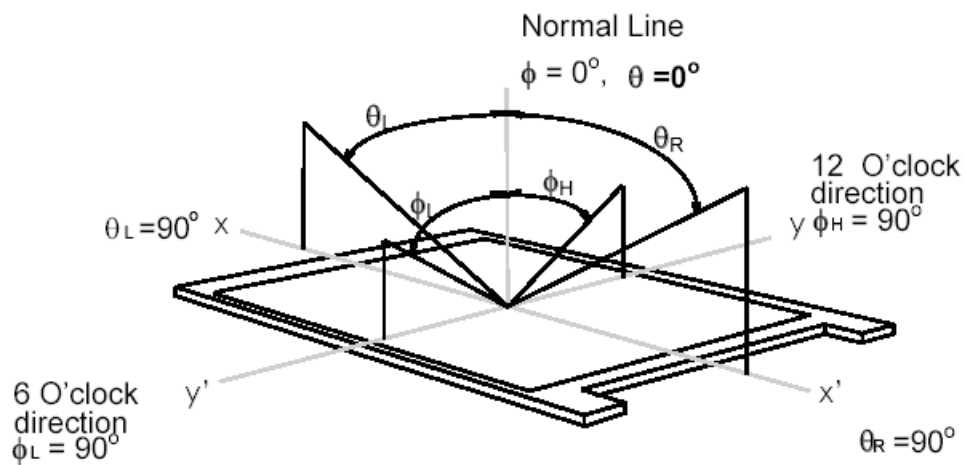
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



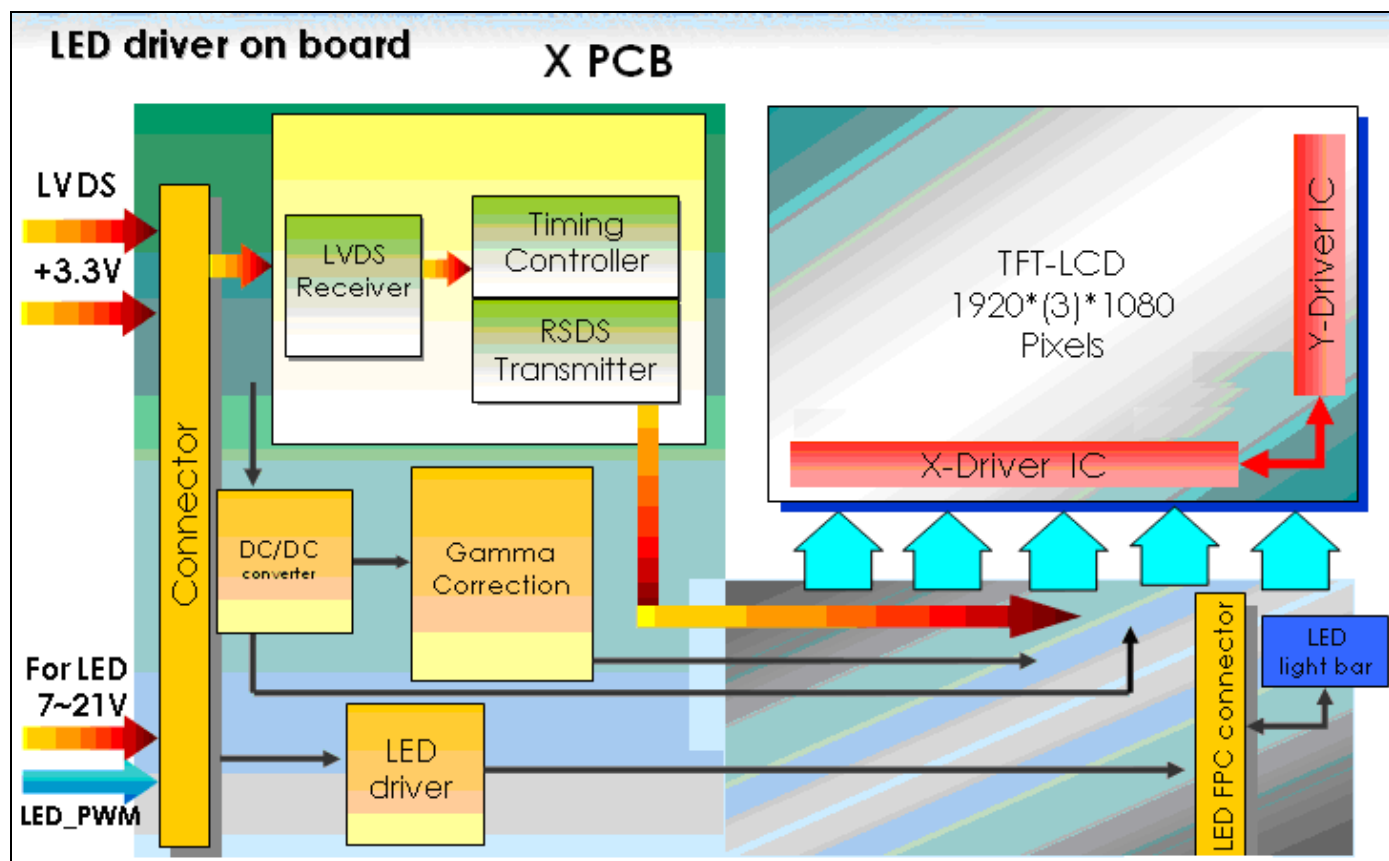
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 40 Pin.



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

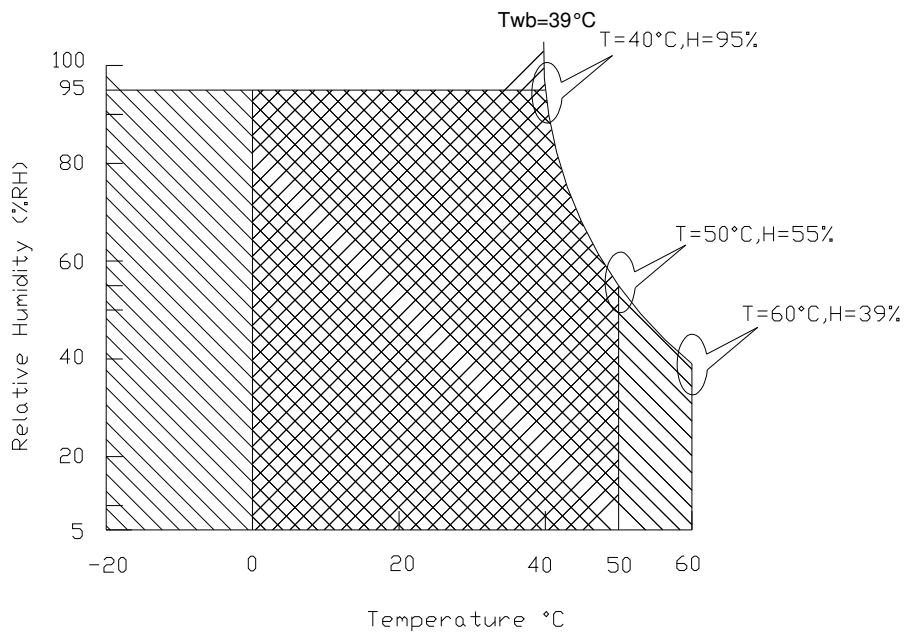
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)



Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

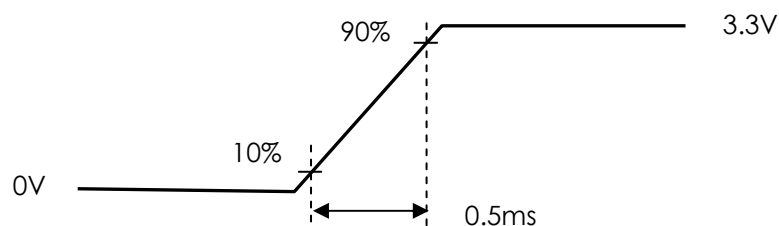
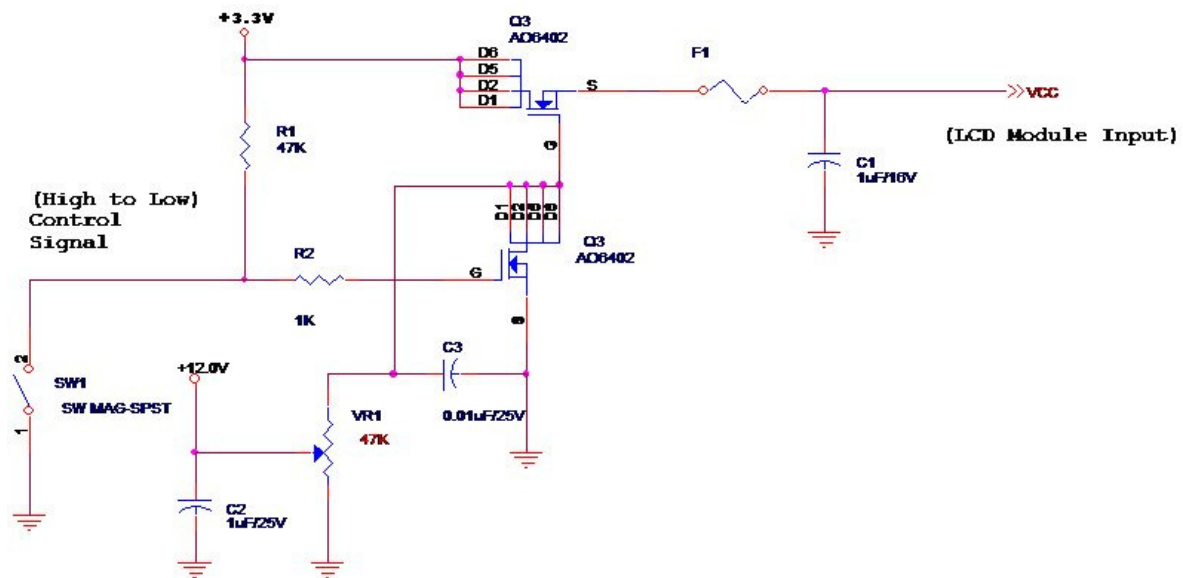
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	2.0	[Watt]	Note 1/2
IDD	IDD Current	-	-	606	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition



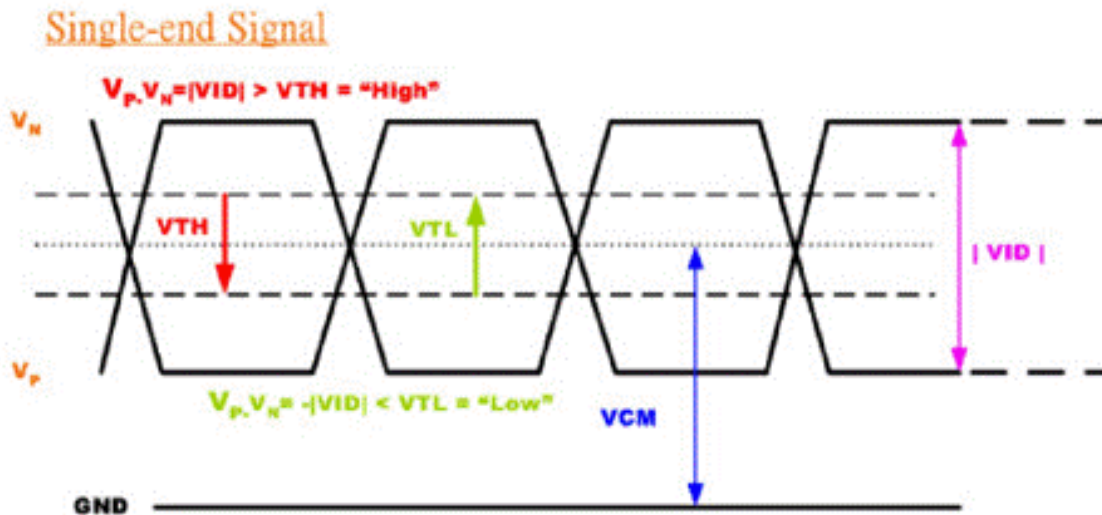
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold ($V_{cm}=+1.2V$)	-	100	[mV]
V_{TL}	Differential Input Low Threshold ($V_{cm}=+1.2V$)	-100	-	[mV]
$ V_{ID} $	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	9.0	9.6	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25°C), Note 2 If=30 mA

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	7.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	200	20k	Hz	
PWM Duty Ratio	Duty	1 *Note 2	--	100	%	

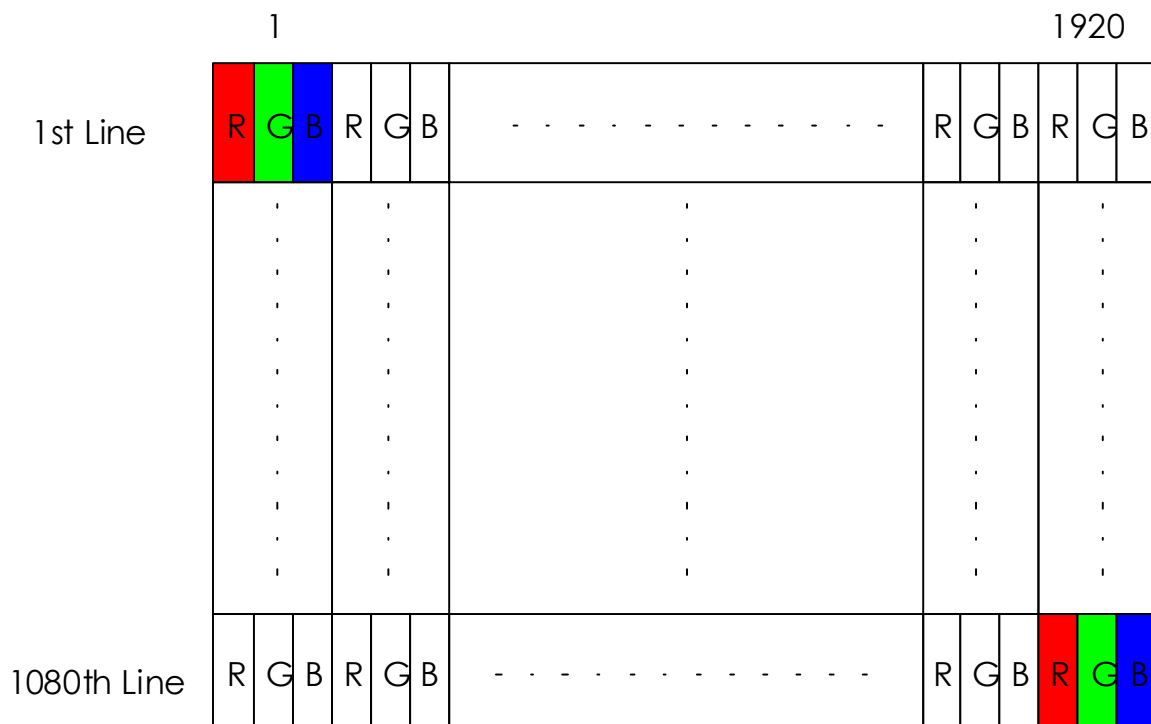
Note 1: Recommended system pull up/down resistor no bigger than 10kohm.

Note 2: If the PWM duty ratio(min) is set between 5% to 1% , the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

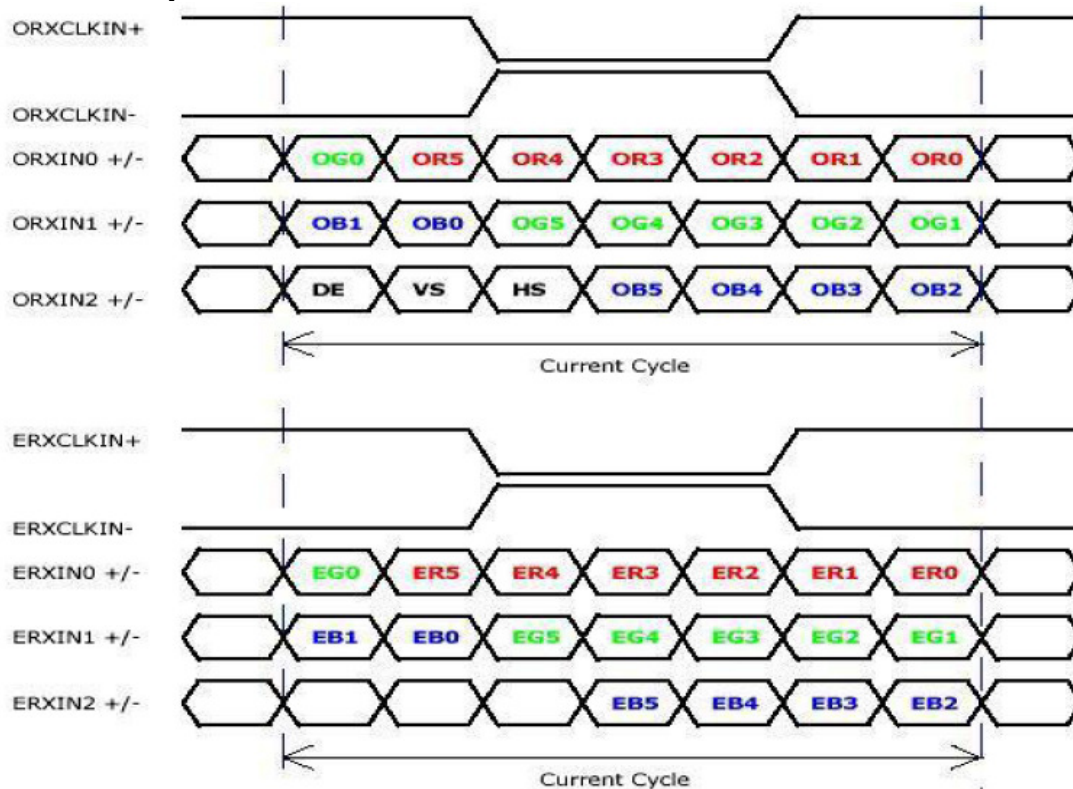
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
	Red-pixel Data	
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
	Green-pixel Data	
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
	Blue-pixel Data	
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



6.3 Integration Interface and Pin Assignment

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	IPEX 20455-040E-#2
Mating Housing/Part Number	IPEX 20353-040T-##

Type / Part Number : #: 0: with datum mark, 1: without datum mark

Mating Housing/Part Number : 1st # (shell-A P/N): 0: with datum mark, 1: without datum mark;

2nd #: 1: with pull bar, 2: without pull bar

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	NC	No Connection (Reserve)
2	AVDD	Power Supply +3.3V
3	AVDD	Power Supply +3.3V
4	DVDD	DDC 3.3Vpower
5	NC	No Connection (Reserve)
6	SCL	DDCClock
7	SDA	DDCData
8	Odd_Rin0-	-LVDS differential data input(R0-R5,G0)
9	Odd_Rin0+	+LVDS differential data input(R0-R5,G0)
10	GND	Ground
11	Odd_Rin1-	-LVDS differential data input(G1-G5,B0-B1)
12	Odd_Rin1+	+LVDS differential data input(G1-G5,B0-B1)
13	GND	Ground
14	Odd_Rin2-	-LVDS differential data input(B2-B5,HS,VS,DE)
15	Odd_Rin2+	+LVDS differential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	Odd_ClkIN	-LVDS differential clock input
18	Odd_ClkIN+	+LVDS differential clock input
19	GND	Ground
20	Even_Rin0-	-LVDS differential data input(R0-R5,G0)
21	Even_Rin0+	+LVDS differential data input(R0-R5,G0)
22	GND	Ground

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6.4 Interface Timing

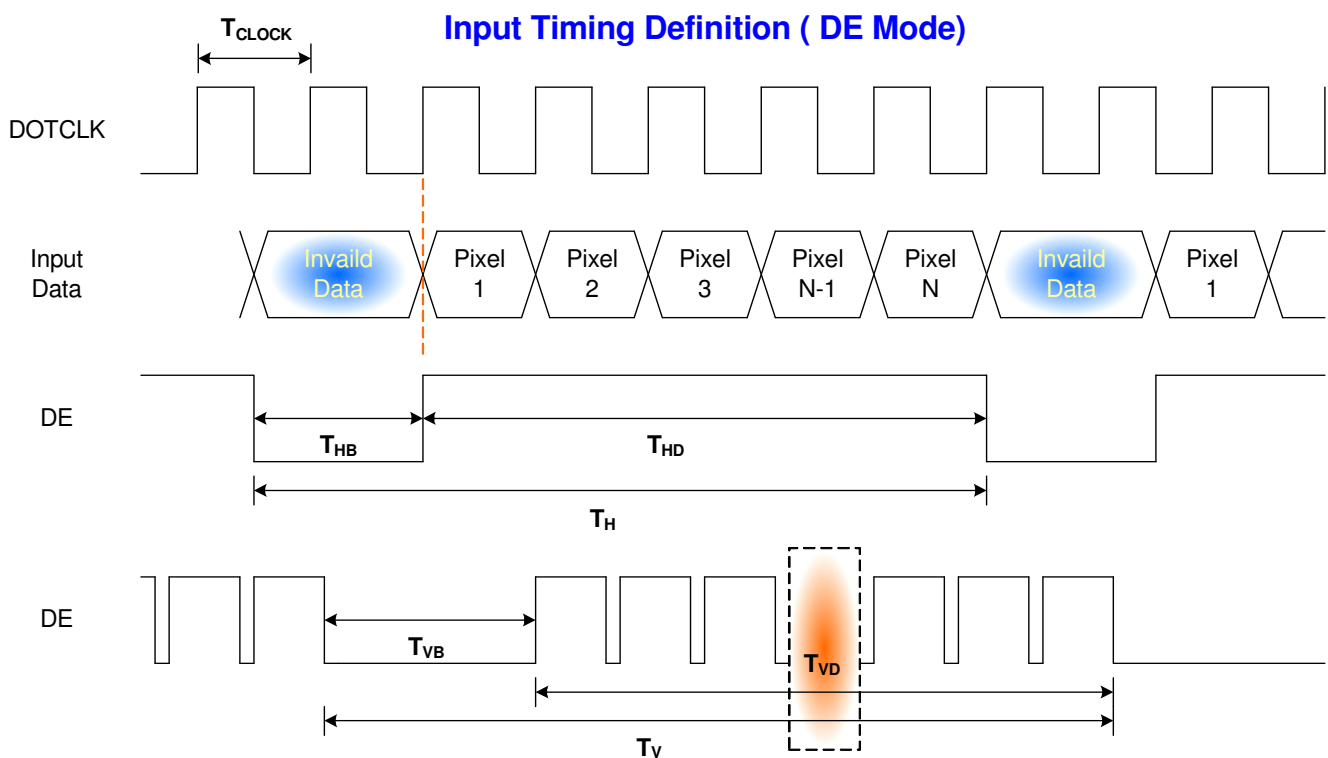
6.4.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	40	60	-	Hz
Clock frequency		1/ T _{Clock}	-	71.19	85	MHz
Vertical Section	Period	T _V	1088	1130	-	T _{Line}
	Active	T _{VD}	1080			
	Blanking	T _{VB}	8	50	-	
Horizontal Section	Period	T _H	990	1050	-	T _{Clock}
	Active	T _{HD}	960			
	Blanking	T _{HB}	30	90	-	

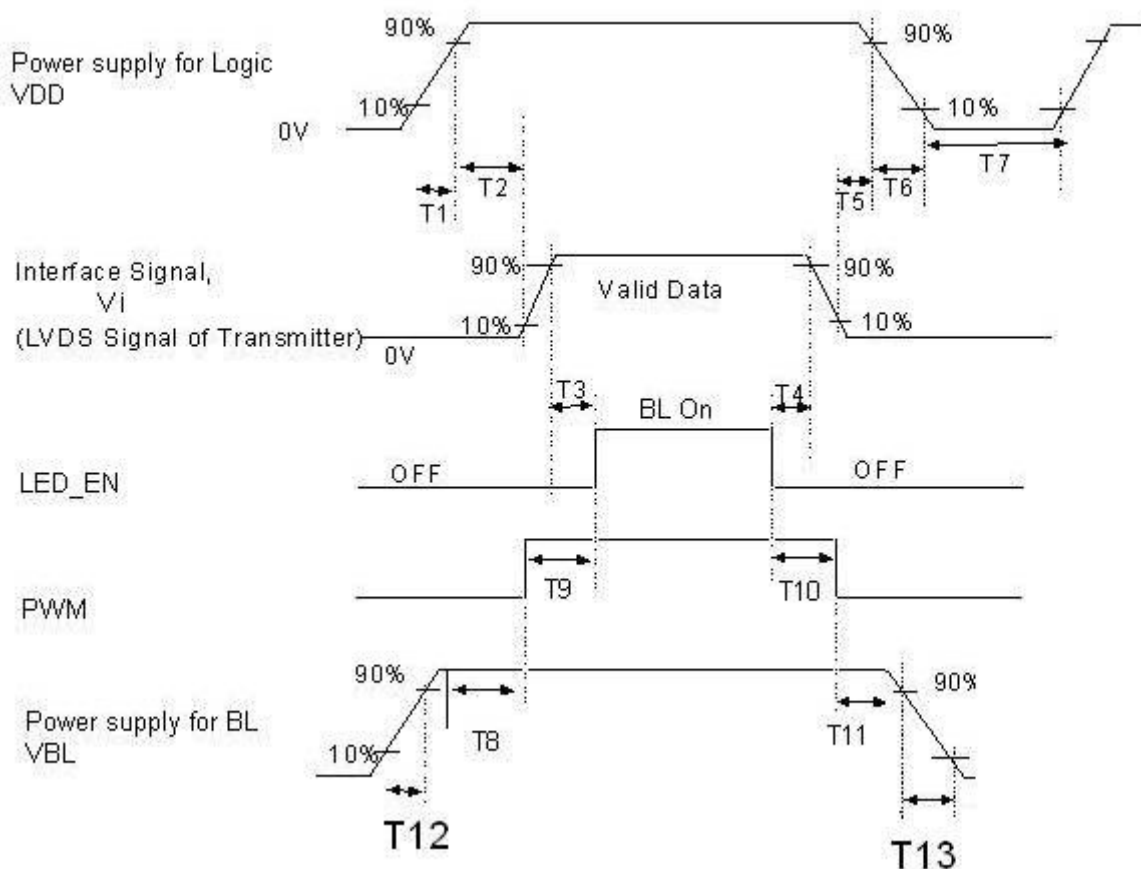
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing				
Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	
T3	200	-	-	
T4	0	-	-	
T5	0	-	-	
T6	0	-	10	
T7	150	-	-	
T8	0	-	-	
T9	0	-	-	
T10	0	-	-	
T11	0	-	-	
T12	0.2	-	-	
T13	0	-	-	

Note: If T4<200ms,the display garbage may occur. We suggest T4>200ms to avoid the display garbage.

Note: If T1 or T12<0.5,the inrush current may cause the damage of fuse If the T1 or T12<0.5,the inrush current I2t is under typical melt of fuse Spec. there's no above-mentioned problem.

Note:If T3,T5,T6 couldn't match above specifications, must request T3+T5+T6 > 200ms at least

7. Vibration and Shock Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃ , 90%RH, 300h	
High Temperature Operation	Ta= 50℃ , Dry, 300h	
Low Temperature Operation	Ta= 0℃ , 300h	
High Temperature Storage	Ta= 60℃ , 35%RH, 300h	
Low Temperature Storage	Ta= -20℃ , 50%RH, 250h	
Thermal Shock Test	Ta=-20℃ to 60℃ , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable.
No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8.1.1 Standard Front View

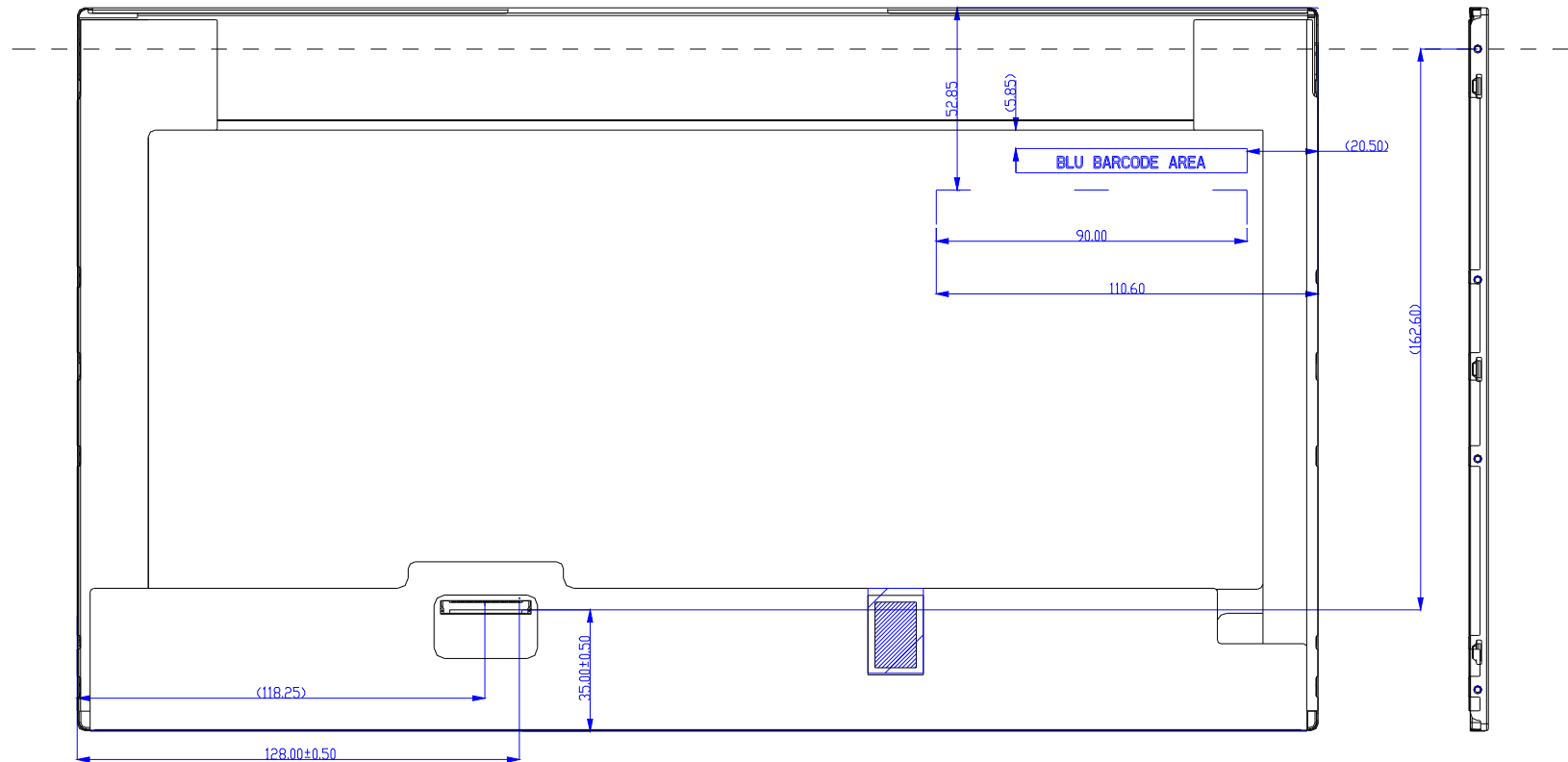




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8.1.2 Standard Rear View



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.



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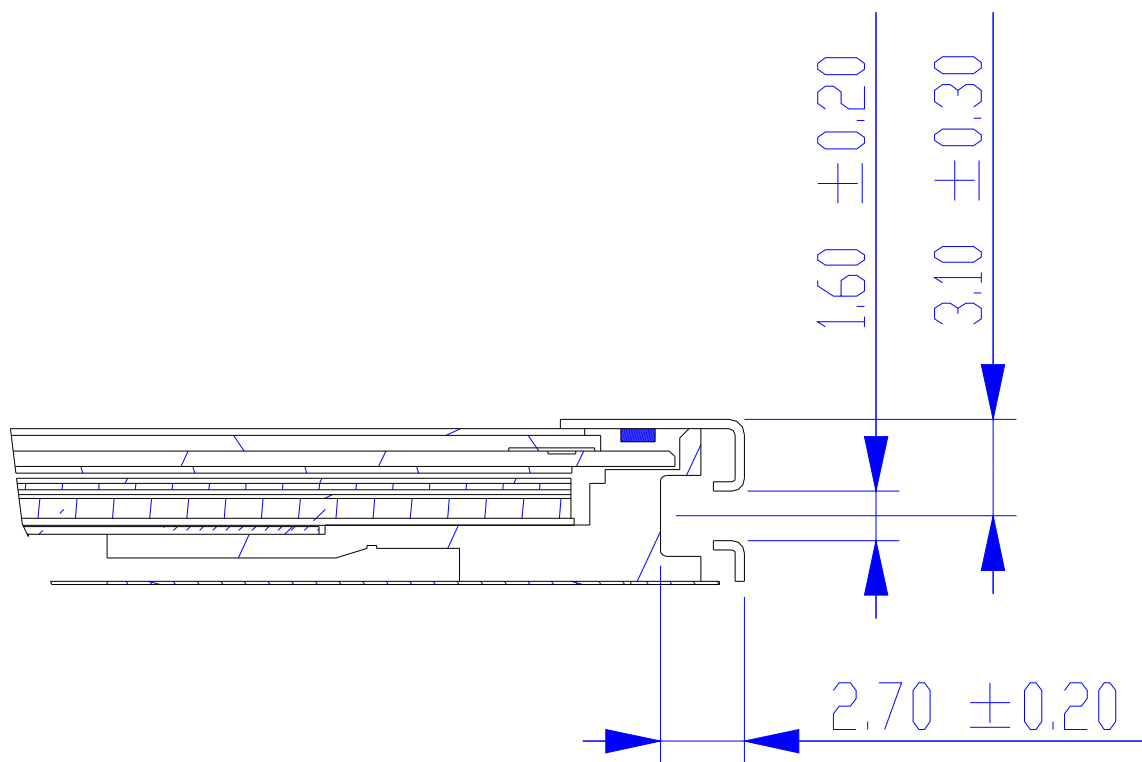
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8.1.3 Screw Hole Depth and Center Position

Maximum Screw penetration from side surface is 2.7 ± 0.2 mm (See drawing)

Screw hole center location, from front surface = 3.10 ± 0.3 mm (See drawing)

Screw Torque: Maximum 2.5 kgf-cm











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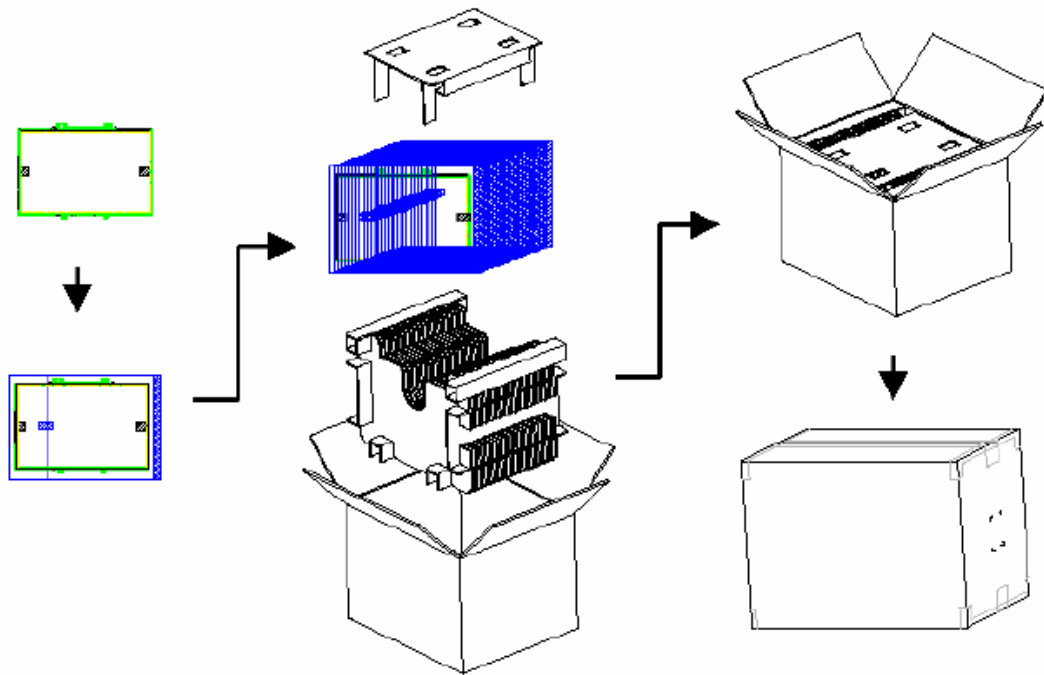
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9. Shipping and Package

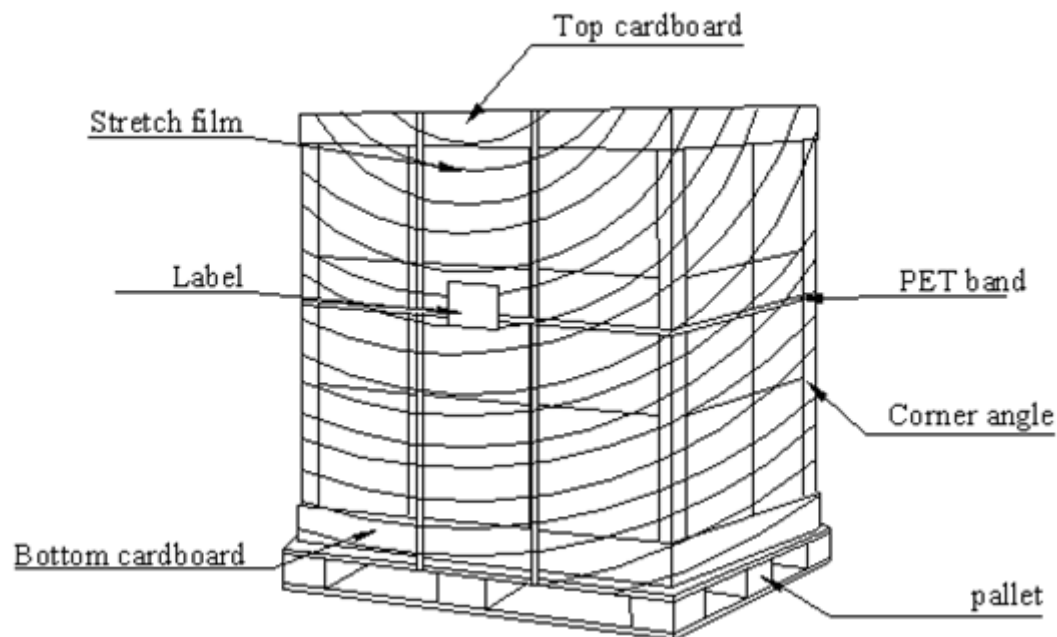
9.1 Shipping Label Format

 XXXXXXXXXXXX-XXXXX	Manufactured MM/WW Model No: B156HTN01.1 AU Optronics MADE IN China (S01) H/W: 0A F/W:1	C  US E204356	
 11S0C00347Z1IN85XXXXXX YMM P/N 0C00347 FRU 04X0609			 

9.2. Carton package



9.3 Shipping package of palletizing sequence





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10. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	0000000 0	0	
01		FF	1111111 1	255	
02		FF	1111111 1	255	
03		FF	1111111 1	255	
04		FF	1111111 1	255	
05		FF	1111111 1	255	
06		FF	1111111 1	255	
07		00	0000000 0	0	
08	EISA Manuf. Code LSB	06	0000011 0	6	
09	Compressed ASCII	AF	1010111 1	175	
0A	Product Code	ED	1110110 1	237	
0B	hex, LSB first	11	0001000 1	17	
0C	32-bit ser #	00	0000000 0	0	Color Engine Setting
0D		00	0000000 0	0	
0E		00	0000000 0	0	
0F		00	0000000 0	0	
10	Week of manufacture	00	0000000 0	0	
11	Year of manufacture	16	0001011 0	22	
12	EDID Structure Ver.	01	0000000 1	1	
13	EDID revision #	04	0000010 0	4	
14	Video input def. (digital I/P, non-TMDS, CRGB)	90	1001000 0	144	
15	Max H image size (rounded to cm)	22	0010001 0	34	
16	Max V image size (rounded to cm)	13	0001001 1	19	
17	Display Gamma (=(gamma*100)-100)	78	0111100 0	120	
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	02	0000001 0	2	
19	Red/green low bits (Lower 2:2:2:2 bits)	21	0010000 1	33	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	35	0011010 1	53	
1B	Red x (Upper 8 bits)	AD	1010110 1	173	
1C	Red y/ highER 8 bits	50	0101000 0	80	
1D	Green x	37	0011011 1	55	
1E	Green y	AA	1010101 0	170	
1F	Blue x	24	0010010 0	36	



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20	Blue y	11	0001000 1	17	
21	White x	50	0101000 0	80	
22	White y	54	0101010 0	84	
23	Established timing 1	00	0000000 0	0	
24	Established timing 2	00	0000000 0	0	
25	Established timing 3	00	0000000 0	0	
26	Standard timing #1	01	0000000 1	1	
27		01	0000000 1	1	
28	Standard timing #2	01	0000000 1	1	
29		01	0000000 1	1	
2A	Standard timing #3	01	0000000 1	1	
2B		01	0000000 1	1	
2C	Standard timing #4	01	0000000 1	1	
2D		01	0000000 1	1	
2E	Standard timing #5	01	0000000 1	1	
2F		01	0000000 1	1	
30	Standard timing #6	01	0000000 1	1	
31		01	0000000 1	1	
32	Standard timing #7	01	0000000 1	1	
33		01	0000000 1	1	
34	Standard timing #8	01	0000000 1	1	
35		01	0000000 1	1	
36	Pixel Clock/10000 LSB	7C	0111110 0	124	
37	Pixel Clock/10000 USB	38	0011100 0	56	
38	Horz active Lower 8bits	80	1000000 0	128	
39	Horz blanking Lower 8bits	D4	1101010 0	212	
3A	HorzAct:HorzBlnk Upper 4:4 bits	70	0111000 0	112	
3B	Vertical Active Lower 8bits	38	0011100 0	56	
3C	Vertical Blanking Lower 8bits	32	0011001 0	50	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	40	0100000 0	64	
3E	HorzSync. Offset	3C	0011110 0	60	
3F	HorzSync.Width	30	0011000 0	48	
40	VertSync.Offset : VertSync.Width	AA	1010101 0	170	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	0000000 0	0	
42	Horizontal Image Size Lower 8bits	58	0101100 0	88	



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43	Vertical Image Size Lower 8bits	C1	1100000 1	193	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	0001000 0	16	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	0000000 0	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	0000000 0	0	
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	0001100 0	24	
48	Detailed timing/monitor	7C	0111110 0	124	
49	descriptor #2	38	0011100 0	56	
4A		80	1000000 0	128	
4B		7E	0111111 0	126	
4C		72	0111001 0	114	
4D		38	0011100 0	56	
4E		32	0011001 0	50	
4F		40	0100000 0	64	
50		3C	0011110 0	60	
51		30	0011000 0	48	
52		AA	1010101 0	170	
53		00	0000000 0	0	
54		58	0101100 0	88	
55		C1	1100000 1	193	
56		10	0001000 0	16	
57		00	0000000 0	0	
58		00	0000000 0	0	
59		18	0001100 0	24	
5A	Detailed timing/monitor	00	0000000 0	0	
5B	descriptor #3	00	0000000 0	0	
5C		00	0000000 0	0	
5D		FE	1111111 0	254	
5E		00	0000000 0	0	
5F	Manufacture	41	0100000 1	65	A
60	Manufacture	55	0101010 1	85	U
61	Manufacture	4F	0100111 1	79	O
62		0A	0000101 0	10	
63		20	0010000 0	32	
64		20	0010000 0	32	
65		20	0010000 0	32	



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66		20	0010000 0	32	
67		20	0010000 0	32	
68		20	0010000 0	32	
69		20	0010000 0	32	
6A		20	0010000 0	32	
6B		20	0010000 0	32	
6C	Detailed timing/monitor	00	0000000 0	0	
6D	descriptor #4	00	0000000 0	0	
6E		00	0000000 0	0	
6F		FE	1111111 0	254	
70		00	0000000 0	0	
71	Manufacture P/N	42	0100001 0	66	B
72	Manufacture P/N	31	0011000 1	49	1
73	Manufacture P/N	35	0011010 1	53	5
74	Manufacture P/N	36	0011011 0	54	6
75	Manufacture P/N	48	0100100 0	72	H
76	Manufacture P/N	54	0101010 0	84	T
77	Manufacture P/N	4E	0100111 0	78	N
78	Manufacture P/N	30	0011000 0	48	0
79	Manufacture P/N	31	0011000 1	49	1
7A	Manufacture P/N	2E	0010111 0	46	.
7B	Manufacture P/N	31	0011000 1	49	1
7C		20	0010000 0	32	
7D		0A	0000101 0	10	
7E	Extension Flag	00	0000000 0	0	
7F	Checksum	81	1000000 1	129	